Quantum Leap Solutions Partner Portfolio

Our Story

Quantum Leap Solutions is a technical sales and advisory firm with established offices in San Jose, Los Angeles, and Austin. Our expertise lies in assisting companies in the completion of their custom silicon designs through a comprehensive suite of IP, EDA, and Services offerings. Our portfolio includes highly reliable and silicon-proven IP offerings available for licensing. Whether you are working on an SOC, ASIC, RFIC, or mixed signal design, we provide compelling solutions tailored to your needs.

Since our inception in 2011, Quantum Leap Solutions has been a trusted provider of IP, design, and manufacturing services for custom IC designs throughout North America. We specialize in delivering semiconductor intellectual property (IP) and design services, offering companies silicon-proven, and low-risk solutions in targeted markets.

Our Partners

ACL Digital

ACL Digital is a global semiconductor services and solutions provider and helps its clients meet market-driven challenges. ACL Digital works closely with several integrated device manufacturers (IDMs), fabless Semiconductor Companies, Original Equipment Manufacturers, Pure Play Foundries, Engineering Design Automation (EDA) and IP vendors to accelerate their products to the market.

With more than 1200 engineers and services from RTL to GDSII, ACL Digital is also a TSMC Design Center Alliance Partner, a RISC-V Center of Excellence, and an ARM Approved Design Partner.

Alphacore

The Alphacore design team has extensive experience in RF or mixed signal intellectual property (IP), including high performance ADC and DACs, specialized imaging systems, hardware-based cybersecurity solutions as well as custom design services.

EnSilica

EnSilica, a UK company founded in 2001, is a fabless ASIC supplier that designs and supplies digital & mixed signal ASICs for automotive/industrial, healthcare and communications markets. EnSilica have ASIC and design expertise in the following application areas: RF & LIDAR/Automotive, Sensing & Control, Communications & Radar, Healthcare & Medical, Satellite RFICs, Digital and DSP, ARM, RISC-V and FuSa applications.

FlexLogix

FlexLogix is a leader in embedded FPGA and AI Inferencing IP. Flex Logix provides eFPGA cores which have density and performance similar to leading FPGAs in the same process node but only use standard cells. FlexLogix EFLX eFPGA is silicon proven in 180nm, 40nm, 28/22nm, 16nm and 12nm with 6/7nm. EFLX eFPGA is in design and 5nm next.

Synopsys

Synopsys is a leading company in the field of Electronic Design Automation and provides a diverse range of Intellectual Property (IP) solutions. In the EDA domain, Synopsys offers tools and software that facilitate the design, verification, and testing of electronic systems, including integrated circuits and semiconductor devices. Their IP portfolio comprises pre-designed and verified blocks of logic, memory, and analog components, enabling semiconductor companies to accelerate the development of their own chips.

ACL Digital has design expertise in the following application areas:
RTL Design & Architecture
Architects – Micro Architects
RTL Front-End Design & Integration
Linting, CDC, Logical Equivalence
RTP Design, IP Design, SoC Integration
UPF Based Low Power Expertise
SoC & IP Verification
IP/SoC Verification
UNM, OVM, VMM, eRM, RVM
Assertion Based Verification
Constraint Random Verification
Power Aware Verification
Formal Verification
AMS Verification
Physical Design
Physical Design (HM, Block, SoC Level)
Scan Insertion, Synthesis and STA
Physical Verification
PPA (Power, Performance, Area Optimization))
Tools and Flow Development
Synthesis and STA
PD Implementation
Low Power Expertise
Design For Test
DFT Design – Hierarchical, Full Flat, Mixed Signal
DFT Implementation – Logic, Memory, IO
DFT Verification – ATPG, MBIST/LBIST BSCAN
Experience in Industry Standard Protocols
FPGA / Prototyping / Hardware
FPGA Based Design and V&V
Experienced Team in Safety Critical Design
Experienced Team in V&V as per DO245 DALs
Emulation – All Major Emulators
ASIC Prototyping
Board Design & Post Silicon
Memory & Analog
Circuit Design & Characterization, Tools & Foundries
Layout Design
View Verification, AMS Modeling & Verification
Memory Compiler Development
Test Chip Development

ALPHACORE Data Converters

Data Converters				Process Technologies				
MSPS	Bits	Type	Architecture	GF55nm	TSMC 28HPC+	GF 22FDx	TSMC 16FFC	TSMC 12FFC
5,000	6	DAC	Current Steering			✓		
10,000	6	ADC	Flash			✓		
20,000	6	ADC	Flash			✓		
40,000	8	ADC	Flash			✓		
160	16	ADC	Pipeline			✓		
500	12	DAC	Current Steering	✓				
6,000	12	DAC	Current Steering			✓		
12,500	6	ADC	Time-Domain Hybrid ADC			✓		
5,000	11	ADC	Hybrid SAR			✓		
400	14	ADC	Hybrid SAR		✓			
200	14	ADC	Hybrid SAR		✓			
400	12	DAC	Current Steering		✓			
200	14	DAC	Current Steering		✓			
4,000	11	ADC	Hybrid SAR		✓			
8,000	11	ADC	Hybrid SAR		✓	✓		
6,000	11	ADC	Hybrid SAR				✓	✓
6,000	14	DAC	Current Steering				✓	✓

ALPHACORE Analog IP

Analog IP		Process Technologies						
Type	**Specs**	**GF55nm**	**TSMC 28HPC+**	**GF 22FDx**	**TSMC 16FFC**	**TSMC 12FFC**	**GF130**	**TSMC 40 ULPe**
PLL: PLL13G	Input Frequency: 40 MHz; Output Frequency: 5.5-13.5 GHz, RMS Jitter: 350fs						✓	
PLL: PLL5G150F	Input Frequency: 100 MHz, 200 MHz; Output Frequency: 5 GHz, RMS Jitter < 150fs			✓				✓
BGR								✓
200 mA Low Dropout Regulator								✓
500 mA Low Dropout Regulator								✓
High-Speed Comparator								✓
Other analog blocks available on request:								
PLLs - please contact QLS for more information								
Temperature Sensor								
Precision Band Gap Reference								
Precision Sample and Hold Amplifier								
Low noise input MUX								
Low-noise Amplifier								
Programmable Gain Amplifier								
Delay Locked Loops								
Pulse Width Modulator								
Samples								
Switches								
Readout Buffer								
Serial Peripheral Interface								

Other capabilities:

- CMOS Image Sensors, Readout ICs, Focal Plane Arrays, Camera Systems, Neuromorphic Imagers
- Power Management ICs for Harsh Environments, DC-DC Converters, Solar Array Interface, LDOs
- Radiation hardened solutions.

EnSilica Mixed Signal ASICS

EnSilica have ASIC and design expertise in the following application areas:
Automotive
H Bridge Solenoid and Motor Controllers
Advanced Radar processing
Video & imagine processing
V2X security and communication
Gas, gyro, position, pressure, force sensor interfacing
Driver monitoring / wellbeing
Battery cell monitoring
Driver monitoring systems (DMS)
ISO 26262
Communications and Radar
Signal processing for satellite and cellular communications systems
High speed interfaces CSI-2, Ethernet, CPRI, PCIe and JESD204B
RF & mmWave RF FE development
Digital beamforming and phases arrays
Base stations and Remote Radio Heads
MIMO systems
Satellite and cellular systems
Industrial
Pressure and flow sensors
Gas sensors
Chemical sensors
Movement and occupancy sensors
Motor and Solenoid controllers
Tags and RFIDs
Inductive speed and position sensors
Precision timers
GaN, Laser and LED drivers
Ultrasonic sensor drivers
Arm safety architectures
ISO 13849-1:2015 & IEC 61508-2:2010
Wearables and Healthcare
Vital signs sensor interfacing monitoring:
• Electrocardiography (ECG)
• Photoplethysmography (PPG)
• Impedance pneumography
• SpO2 measurement
• Near infra-red spectroscopy (NIRS)

• Fluorescent glucose sensing (non-invasive to body tissue)
• Body temperature sensors
Electrochemical sensor interfacing
Differential capacitive sensors
Hearing aids
Lab-on chip interfaces
Designing and integrating wireless interfaces including NFC/RFID and BLE
Satellite RFICs
Ka band suitable for GEO, LEO
17.2 to 21.2 GHz Rx
27.5 to 30.0 GHz Tx
4 Rx element paths
4 Tx element paths
Ka-band fine gain and phase control
Integrated IQ frequency conversion
Comprehensive and flexible IQ IF/BB path to data converters
Low power operation VDDRF=1.1V
Logic at 1.8V
Support for large arrays
Analog, hybrid & digital beamforming
Small size WLCSP
Digital and DSP
Systems/DSP expertise include
Modem design – BLE/DVB/DAB/WiFi
Remote Radio Heads - DDC/DUC
Advanced MIMO processing and beamforming
Advanced Radar signal processing
Cryptography
Development of efficient data-path designs
Integration of high-speed interfaces
PCIe, USB, MIPI, CSI-2, CPRI, 1/25/10Gb Ethernet, LPDDR/DDR
Processor integration
Cores - Arm, Cadence Tensilica, MIPS
AMBA - AHB/AXI/APB
Advanced Verification
Constrained random SV based verification using UVM and VIPs
Embedding system models in environment using MATLAB/SystemC
FPGA based prototyping / emulation
Post silicon validation
Bit accurate models and GPU acceleration in CUDA
Embedded software
DSP and embedded software development for Arm, TenSilica, GPUs
Linux drivers and BSP
Physical design

FlexLogix eFPGAs

FlexLogix EFLX Provides Fast Flexible Computing

- Mature Solutions
  - Flexible Architecture and Sizing
  - Dynamically Reconfigurable eFPGA in useconds
  - RAD Hardened Capable
- High Density, High Performance and Low Power
  - Area and Utilization Leading Technology
  - Supported on Multiple Popular Processes
  - Optimized Functionality for Low Power
- Software Tool Chain
  - Power Estimator
  - On Chip Debug

EFLX eFPGA Availability			
TSMC	**Product**	**Logic**	**DSP**
40 ULP/EF*/LP*	EFLX 1K w/Power Gating	Silicon Proven	On Demand
28 HPC/HPC+	EFLX 4K	Silicon Proven	Silicon Proven
16 FFC/FFC+	EFLX 4K	Silicon Proven	Silicon Proven
12 FFC/FFC+	EFLX 4K	Silicon Proven	Silicon Proven
N7/N6	EFLX 4K	Available	Available
NS	EFLX 4K	*In Planning*	*In Planning*
Global Foundries			
22 FDX	EFLX 4K	In Design**	In Design**
12 LP/LP+	EFLX 4K	Silicon Proven	Silicon Proven
12LP LP	EFLX 4K w/Power Gating	Silicon Proven	Silicon Proven
12LP RHBD	EFLX 4K	Silicon Proven	Silicon Proven
Other			
Sandia 180 RHBD	EFLX 4K	Silicon Proven	
Samsung 14LPP*	EFLX 4K	Available	Available

* Available. Re-timing Required

** Early IP drops available for concurrent design

Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate IP integration, software development, and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, pre-verified and customizable IP subsystems, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

Interface IP	Analog IP	Foundation IP	SLM Monitors IP	Security IP	Processor IP	IP Subsystems
Die-to-Die	Data Converters	Embedded Memories	Path Margin Monitor IP	Security	ARC VPX DSP Processors	Interface IP Subsystems
PCIe		Logic Libraries			ARC NPX Neural Processors	Interface IP Subsystems
Ethernet		I/O Products			Embedded Vision Processors	Configurable IP Subsystems
HBM		Non-Volatile Memory			ARC HS 32-bit Processors	
DDr		In-Chip PVT Monitoring IP			ARC 32-bit Processors	
CXL					ARC Processor IP Subsystems	
CCXL						
USB						
MPI						
Embedded Flash Storage						
HDMI / DisplayPort						
Bluetooth, Thread, Zigbee						
SATA						
AMBA						
Datapath IP						

Synopsys EDA Products

Synopsys offers an advanced and comprehensive software flow tailored to meet the complex demands of semiconductor chip and SoC designers. This flow encompasses a series of interconnected tools and methodologies that collectively enable efficient design, verification, and deployment of SoCs, which integrate multiple components and functionalities onto a single chip.

Throughout the entire design flow, Synopsys' suite of software tools aims to provide a comprehensive and cohesive solution to address the various challenges of designing complex chips. The integration of these tools helps streamline the design process, improve design quality, and reduce time-to-market for innovative designs.

Below is a listing of Synopsys EDA-Software Anchor Products

Design Planning and System Architecture

The flow begins with defining the high-level architecture and design specifications for the chip. Synopsys provides tools for creating functional and performance models, as well as architectural exploration tools to optimize the design for power, performance, and area.

- ***3DIC Compiler***: The Synopsys 3DIC Compiler platform is a complete, end-to-end solution for efficient, 2.5D, and 3D multi-die system integration.
- ***Platform Architect***: Provides architects and system designers with SystemC™ TLM-based tools and efficient methods for early analysis and optimization of multicore SoC architectures for performance and power.

Design Capture and Synthesis

Register Transfer Level (RTL) design involves creating the digital logic description of the chip. Synopsys tools aid in RTL coding, verification, and synthesis, converting the design into gates and optimizing it for power, performance, and area.

- ***Design Compiler***: Handles RTL coding, synthesis, and optimization for power, performance, and area.
- ***Fusion Compiler***: Fusion Compiler features a unique RTL-to-GDSII architecture that enables customers to reimagine what is possible from their designs and take the fast path to achieving maximum differentiation.
- ***Custom Compiler***: As the heart of the Synopsys Custom Design Family, Custom Compiler provides design entry, simulation management and analysis, and custom layout editing features.

Verification

Ensuring the correctness of the design is paramount. Synopsys' verification tools encompass simulation, emulation, and formal verification techniques. They help identify and resolve functional errors and ensure the design behaves as expected.

- ***VCS*** (Verilog Compiler Simulator): A high-performance simulation tool for verifying the correctness of the design.
- ***VC SpyGlass***: Synopsys VC SpyGlass integrates advanced algorithms and analysis techniques that provides designers detailed information and insights about their design much earlier in the RTL phase.
- ***Verdi***: Enables comprehensive debug for all design and verification flows. It includes powerful technology that helps you comprehend complex and unfamiliar design behavior, automate difficult and tedious debug processes and unify diverse and complicated design environments.
- ***VSO.ai: Synopsys VSO.ai***™ (Verification Space Optimization) delivers the industry's first AI-driven verification solution to help verification teams achieve coverage closure faster and with higher quality.
- ***PrimeSim***: PrimeSim™ SPICE is a high-performance SPICE circuit simulator for analog, RF, and mixed-signal applications.

Implementation

This stage involves translating the logical design into a physical layout. Synopsys tools assist in floorplanning, placement, routing, and chip assembly, optimizing for manufacturability and performance.

- ***Fusion Compiler***: Fusion Compiler features a unique RTL-to-GDSII architecture that enables customers to reimagine what is possible from their designs and take the fast path to achieving maximum differentiation.
- ***DSO.ai***: DSO.ai searches for optimization targets in very large solution spaces of chip design, utilizing reinforcement learning to enhance power, performance, and area.
- ***Custom Compiler***: As the heart of the Synopsys Custom Design Family, Custom Compiler provides design entry, simulation management and analysis, and custom layout editing features.

Analog/Mixed Signal Design

- ***Custom Compiler***: Tool for custom layout design of analog and mixed-signal circuits.
- ***PrimeSim HSPICE***: PrimeSim HSPICE is the industry's 'gold standard' for accurate circuit simulation and offers foundries-certified MOS device models with state-of-the-art simulation and analysis algorithms.

Signoff

Synopsys' design analysis and signoff solution includes a broad portfolio of products for static timing analysis, advanced signal integrity, power and power integrity, parasitic extraction, ECO closure, transistor-level analysis and library characterization.

- ***PrimeTime***: Enables power analysis and optimization.
- ***PrimePower***: Power analysis tool for estimating power consumption and optimizing power distribution networks.
- ***StarRC***: The StarRC™ solution is the EDA industry's gold standard for parasitic extraction.
- ***IC Validator***: Synopsys IC Validator™ physical verification high-performance signoff solution improves productivity for customers at all process nodes, from mature to advanced.

Silicon Test & Lifecycle Management

Synopsys integrated Silicon Lifecycle Management (SLM) family of products improves silicon health and operational metrics at every phase of the device lifecycle. Synopsys SLM family of products is built on a foundation of enriched in-chip observability, analytics and integrated automation. Monitors enable deep insights from silicon to system. Meaningful data is gathered at every opportunity for continuous analysis and actionable feedback.

- ***TestMAX***: The Synopsys TestMAX™ family of products offers innovative, next-level test and diagnosis capabilities for all digital, memory and analog portions of a semiconductor device.
- ***DFT/ATPG***: ATPG is Synopsys' state-of-the-art pattern generation solution that enables design teams to meet their test quality and cost goals with unprecedented speed.
- ***TSO.ai***: TSO.ai automatically searches for an optimal solution in a large test search space to minimize pattern count and ATPG turn-around time reducing test costs dramatically.
- ***PVT Sensors***: As the name implies, PVT sensors represent embedded analog IP blocks that are typically integrated into SoCs with the goal of sensing the process variability and operating environment of the chip. These devices exploit the fact that certain measurable characteristics of a semiconductor device change depending on levels of activity, due to variable software operation or CPU loading, and also from environmental conditions.
- ***Path-Margin IP***: Path selection logic, RTL configuration and generation, connecting to functional and/or test paths, synthesis, implementation, timing validation and path qualification are the key functions addressed by the EDA automation provided.

Prototyping and Emulation

Synopsys tools enable the creation of FPGA-based prototypes and hardware emulators for early software development and system validation.

- ***HAPS Prototyping Solution***: Enables FPGA-based prototypes for software development and system validation.
- ***Zebu Server***: Provides hardware emulation capabilities.

TCAD, OPC, Smart Manufacturing

The smart manufacturing solutions from Synopsys are built upon Synopsys' extensive expertise in IC design, mask synthesis, process modeling, on-chip test and monitoring techniques and cloud-based data analytics.

- ***Proteus OPC***: achieve exceptional precision, efficiency and speed in proximity correction, model building for correction, and analyzing proximity effects on corrected and uncorrected IC layout patterns, revolutionizing your chip fabrication process.
- ***Sentaurus***: Sentaurus Process is an advanced 1D, 2D and 3D process simulator for developing and optimizing silicon semiconductor process technologies.
- ***TCAD***: Synopsys TCAD offers a comprehensive suite of products that includes industry-leading process and device simulation tools, as well as a powerful graphical user interface (GUI) driven simulation environment for managing simulation tasks and analyzing simulation results.
- ***BISTel Yield Management***: BISTel solutions collect, manage, and analyze data, monitor the health of equipment, optimize process flows, identify the root cause of failures rapidly, and predict outcomes to mitigate manufacturing risks.